What Is Claimed Is:

1. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region;

a thin film transistor connected to the gate line and the data line;

a common line parallel to and spaced apart from the gate line;

a common electrode extending from the common line and including a plurality of common electrode patterns;

a pixel connecting line connected to a capacitor electrode; and

a pixel electrode extending from the pixel connecting line and including a plurality of pixel electrode patterns,

wherein one of the plurality of common electrode patterns and one of the plurality of pixel electrode patterns form concentric rings of pixel and common electrode patterns that are within an open region of another one of the plurality of common electrode patterns.

2. The array substrate of claim 1, wherein another one of the plurality of pixel electrode patterns is a circular shape at the center of the pixel region.

3. The array substrate of claim 1, wherein the open region of another one of the plurality of common electrode patterns has a substantially rectangular shape.

4. The array substrate of claim 1, wherein the open region of another one of the plurality of

common electrode patterns has a substantially circular shape.

5. The array substrate of claim 1, wherein the pixel region has a square shape.

6. The array substrate of claim 5, wherein neighboring four pixel regions correspond to red, green, blue and white colors, respectively.

7. The array substrate of claim 1, further comprising a black matrix having an opening larger than the open region of another one of the plurality of common electrode patterns.

8. The array substrate of claim 1, wherein the capacitor electrode and the another one of the plurality of common electrode patterns overlap each other and constitute a first storage capacitor.

9. The array substrate of claim 8, wherein the capacitor electrode overlaps a previous gate line in a neighboring pixel region and constitutes a second storage capacitor.

10. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line and defining a pixel region;

a thin film transistor including a drain electrode and connected to the gate line and the data line;

a common line parallel to and spaced apart from the gate line;

a pixel connecting line extending from the drain electrode;

a common electrode contacting the common line and including a plurality of common electrode patterns; and

a pixel electrode contacting the pixel connecting line and including a plurality of pixel electrode patterns,

wherein one of the plurality of common electrode patterns has two symmetric half-ring shaped portions and one of the plurality of pixel electrode patterns has two symmetric half-ring shaped portions that are concentrically arranged within an open region of another one of the plurality of common electrode patterns.

11. The array substrate of claim 10, wherein another one of the plurality of pixel electrode patterns is a circular shape at the center of the pixel region.

12. The array substrate of claim 10, wherein the open region of another one of the plurality of common electrode patterns has a substantially rectangular shape.

13. The array substrate of claim 10, wherein the pixel region has a square shape.

14. The array substrate of claim 13, wherein neighboring four pixel regions correspond to red, green, blue and white colors, respectively.

15. The array substrate of claim 10, further comprising a black matrix having an opening larger than the open region of another one of the plurality of common electrode patterns.

16. The array substrate of claim 10, wherein the capacitor electrode and the another one of the plurality of common electrode patterns overlap each other and constitute a first storage capacitor.

17. The array substrate of claim 10, wherein the common electrode and the pixel electrode are formed of the same material.

18. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line and defining a pixel region;

a thin film transistor including a drain electrode and connected to the gate line and the data line;

a common line parallel to and spaced apart from the gate line;

a pixel connecting line extending from the drain electrode;

a passivation layer having first and second contact holes on the pixel connecting line, the first contact hole exposing the common electrode and the second contact hole exposing the pixel connecting line;

a common electrode contacting the common line through the first contact hole and including a plurality of common electrode patterns; and

a pixel electrode contacting the pixel connecting line through the second contact hole and including a plurality of pixel electrode patterns,

wherein one of the plurality of common electrode patterns and one of the plurality of pixel electrode patterns form concentric rings of pixel and common electrode patterns that are

within an open region of another one of the plurality of common electrode patterns.

19. The array substrate of claim 18, wherein another one of the plurality of pixel electrode patterns is a circular shape at the center of the pixel region.

20. The array substrate of claim 18, wherein the open region of another one of the plurality of common electrode patterns has a substantially rectangular shape.

21. The array substrate of claim 18, wherein the common electrode and pixel electrode are formed of the same material.

22. The array substrate of claim 18, wherein the pixel region has a substantially square shape.

23. The array substrate of claim 22, wherein neighboring four pixel regions correspond to red, green, blue and white colors, respectively.

24. The array substrate of claim 18, further comprising a black matrix having an opening larger than the open region of another one of the plurality of common electrode patterns.

25. The array substrate of claim 18, wherein the pixel connecting line overlaps the common electrode and constitutes a first storage capacitor.

26. The array substrate of claim 25, wherein the pixel connecting line overlaps a previous

gate line in a neighboring pixel region and constitutes a second storage capacitor.

27. The array substrate of claim 18, wherein the another one of the plurality of common electrode patterns covers the data line.

28. The array substrate of claim 18, wherein the passivation layer includes one of benzocyclobutene and acrylic resin.

29. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line and defining a pixel region;

a thin film transistor including a drain electrode and connected to the gate line and the data line;

a common line parallel to and spaced apart from the gate line;

a common electrode extending from the common line and including first and second common electrode patterns; and

a pixel electrode extending from the drain electrode and including first and second pixel electrode patterns,

wherein the first common electrode pattern has corner portions and defines an open region that has a substantially rectangular shape, and the second common electrode pattern has a spiral shape and the second pixel electrode pattern has a spiral shape.

30. The array substrate of claim 29, wherein the second common electrode pattern is

intertwined with the second pixel electrode pattern.

31. The array substrate of claim 29, wherein the pixel region has a square shape.

32. The array substrate of claim 31, wherein neighboring four pixel regions correspond to red, green, blue and white colors, respectively.

33. The array substrate of claim 29, further comprising a black matrix having an opening larger than the open region in the first common electrode pattern.

34. The array substrate of claim 29, wherein the first pixel electrode pattern overlaps the common electrode and constitutes a first storage capacitor.

35. The array substrate of claim 34, wherein the first pixel electrode pattern overlaps a previous gate line in a neighboring pixel region and constitutes a second storage capacitor.

36. The array substrate of claim 29, further comprising a pixel connecting line connected to the capacitor electrode.

37. A method of fabricating an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns and a common line parallel to and spaced apart from the gate line on

a substrate through a first mask process;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a data line crossing the gate line and defining a pixel region, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode and a semiconductor layer corresponding to the data line, the source electrode and the drain electrode through a second mask process, the semiconductor layer being exposed between the source and drain electrodes, the gate electrode, the semiconductor layer, the source electrode and the drain electrode constituting a thin film transistor;

forming a passivation layer on the thin film transistor through a third mask process, the passivation layer having a drain contact hole exposing the drain electrode; and

forming a capacitor electrode overlapping the common electrode and being connected to the drain electrode, a pixel connecting line connected to the capacitor electrode and a pixel electrode extending from the pixel connecting line and including a plurality of pixel electrode patterns on the passivation layer through a fourth mask process,

wherein one of the plurality of common electrode patterns and one of the plurality of pixel electrode patterns form concentric rings of pixel and common electrode patterns that are within an open region of another one of the plurality of common electrode patterns.

38. The method of claim 37, further comprising forming a black matrix having an opening larger than the open region of another one of the plurality of common electrode patterns.

39. A method of fabricating an array substrate for an in-plane switching liquid crystal display

device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns and a common line parallel to and spaced apart from the gate line on a substrate through a first mask process;

forming a gate insulating layer on the gate line, the common electrode and the common line;

forming a data line crossing the gate line to define a pixel region, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode, a pixel connecting line extending from the drain electrode, a capacitor electrode extending from the pixel connecting line and a semiconductor layer corresponding to the data line, the source electrode, the drain electrode, the pixel connecting line and the capacitor electrode through a second mask process, the semiconductor layer being exposed between the source and drain electrodes, the gate electrode, the semiconductor layer, the source electrode and the drain electrode constituting a thin film transistor;

forming a photoresist pattern on the thin film transistor through a third mask process, the photoresist pattern corresponding to a plurality of regions between the plurality of common electrode patterns;

forming a conductive layer on an entire surface of the substrate having the photoresist pattern; and

removing the conductive layer on the photoresist pattern by stripping the photoresist pattern to obtain a pixel electrode contacting the pixel connecting line and including a plurality of pixel electrode patterns,

wherein one of the plurality of common electrode patterns and one of the plurality of

pixel electrode patterns form concentric rings of pixel and common electrode patterns that are within an open region of another one of the plurality of common electrode patterns.

40. The method of claim 39, wherein the conductive layer is formed of indium tin oxide (ITO).

41. A method of fabricating an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode and a common line parallel to and spaced apart from the gate line on a substrate through a first mask process;

forming a gate insulating layer on the gate line and the common line;

forming a data line crossing the gate line to define a pixel region, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode, a pixel connecting line extending from the drain electrode, a capacitor electrode extending from the pixel connecting line and a semiconductor layer corresponding to the data line, the source electrode, the drain electrode, the pixel connecting line and the capacitor electrode through a second mask process, the semiconductor layer being exposed between the source and drain electrodes, the gate electrode, the semiconductor layer, the source electrode and the drain electrode constituting a thin film transistor;

forming a photoresist pattern on the thin film transistor through a third mask process, the photoresist pattern including first two symmetric open portions separated from the pixel connecting line and second two symmetric open portions separated from the common line;

etching the gate insulating layer using the photoresist pattern as an etch mask to expose

the common line;

forming a conductive layer on an entire surface of the substrate having the photoresist pattern; and

removing the conductive layer on the photoresist pattern by stripping the photoresist pattern to obtain a common electrode contacting the common line and including a plurality of common electrode patterns and a pixel electrode contacting the pixel connecting line and including a plurality of pixel electrode patterns,

wherein the plurality of common electrode patterns and the plurality of pixel electrode patterns include two symmetric portions having a concentric half-ring shape except for an outermost common electrode pattern and an inmost common electrode patterns,

wherein each common electrode pattern is separated from the pixel connecting line and each pixel electrode pattern is separated from the common line,

wherein the outermost common electrode pattern has a half-rectangular shape including corner portions and the inmost common electrode pattern is formed inside a region corresponding to the pixel connecting line.

42. The method of claim 41, wherein the conductive layer is formed of one of indium tin oxide (ITO) and indium zinc oxide (IZO).

43. A method of fabricating an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common line parallel to and spaced apart from the gate line, a common electrode extending from the common line and including first and

second common electrode patterns on a substrate through a first mask process;

forming a gate insulating layer on the gate line, the common line and the common electrode;

forming a data line crossing the gate line to define a pixel region, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode and a semiconductor layer corresponding to the data line, the source electrode, the drain electrode on the gate insulating layer through a second mask process, the semiconductor layer being exposed between the source and drain electrodes, the gate electrode, the semiconductor layer, the source electrode and the drain electrode constituting a thin film transistor;

forming a passivation layer having a drain contact hole on the thin film transistor through a third mask process, the drain contact hole exposing the drain electrode; and

forming a pixel electrode connected to the drain electrode through the drain contact hole and including first and second pixel electrode patterns through a fourth mask process,

wherein the first common electrode pattern has a rectangular shape including corner portions,

wherein the second common electrode pattern and the second pixel electrode pattern have a spiral shape.

44. A method of fabricating an array substrate for an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode and a common line parallel to and spaced apart from the gate line on a substrate;

forming a gate insulating layer on the gate line and the common line;

forming a data line crossing the gate line and defining a pixel region, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode, a pixel connecting line connected to the drain electrode, and a semiconductor layer corresponding to the data line, the source electrode and the drain electrode, the semiconductor layer being exposed between the source and drain electrodes, the gate electrode, the semiconductor layer, the source electrode and the drain electrode constituting a thin film transistor;

forming a passivation layer on the thin film transistor, the passivation layer having a first contact hole exposing the common line and a second contact hole exposing the pixel connecting line;

forming a plurality of common and pixel electrodes on the passivation layer,

wherein the plurality of common and pixel electrodes are formed of concentric rings, the common electrodes connected to the common line through the first contact hole, and the pixel electrode connected to the pixel connecting line through the second contact hole.

45. The method of claim 44, wherein the common and pixel electrodes are formed of indium tin oxide (ITO).

46. The method of claim 44, wherein one of the common electrodes overlaps a portion of the data line.

47. An array substrate for an in-plane switching liquid crystal display device, comprising:

a gate line on a substrate;

a data line crossing the gate line to define a pixel region having an aperture area;

a gate pad connected to one end of the gate line;

a data pad connected to one end of the data line;

a gate pad terminal connected to the gate pad;

a data pad terminal connected to the data pad;

a semiconductor line under the data line and having the same pattern shape as the data line;

a thin film transistor disposed at one corner of the pixel region and connected to the gate and data lines, the thin film transistor including source and drain electrodes and a semiconductor layer extending from the semiconductor line;

a common line spaced apart from and substantially parallel to the gate line;

a common electrode extending from the common line and including a plurality of common electrode patterns, wherein an outermost common electrode pattern is substantially rectangle-shaped within the pixel region and has a substantially rectangular opening in the middle thereof;

a capacitor electrode overlapping a previous gate line of a previously neighboring pixel region;

a pixel electrode within the substantially rectangular opening and including a plurality of pixel electrode patterns; and

a pixel connecting line substantially parallel to the data line in the pixel region and connected to the capacitor electrode, the pixel electrode and the drain electrode of the thin film transistor,

wherein the innermost pixel electrode pattern is shaped like a rod and disposed within an area of the pixel connecting line,

wherein the pixel electrode overlaps portions of the pixel connecting line and directly contacts the pixel connecting line,

wherein other pixel electrode patterns are patterned to have semicircular shapes, and

wherein the semiconductor line extends underneath the source and drain electrodes, the pixel connection line and the capacitor electrode,

wherein an innermost portion of the plurality of common electrode patterns is substantially circular band shaped, and

wherein the aperture area is circular band shaped.

48. The array substrate of claim 47, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

49. The array substrate of claim 47, wherein the innermost portion of the pixel electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

50. The array substrate of claim 48, wherein the capacitor electrode pattern is connected to the thin film transistor though the pixel connecting line.

51. The array substrate of claim 48, wherein four neighboring pixel regions correspond to red, green, blue and white colors, respectively.

52. The array substrate of claim 48, wherein the pixel and common electrode patterns are

disposed within the substantially circular opening, except the outermost common electrode pattern.

53. A method of forming an array substrate for use in an in-plane switching liquid crystal display device, comprising:

forming a gate line having a gate electrode, a common electrode including a plurality of common electrode patterns, a gate pad connected to one end of the gate line and a common line substantially parallel to and spaced apart from the gate line on a substrate using a first mask process, wherein an outermost common electrode pattern is substantially rectangle-shaped and has a substantially rectangular opening in the middle thereof;

forming a gate insulating layer on the gate line, the common electrode, the gate pad and the common line;

forming a data line that crosses the gate line to define a pixel region having an aperture area, a source electrode extending from the data line, a drain electrode spaced apart from the source electrode across the gate electrode, a pixel connecting line extending from the drain electrode and substantially parallel to the data line, a capacitor electrode over a previous gate line with extending from the pixel connecting line, a data pad connected to one end of the data line, a semiconductor line under the data line and having the same pattern shape with the data line, and a semiconductor layer extending from the semiconductor line over the gate electrode and under the source and drain electrodes and pixel connecting line and capacitor electrode using a second mask process, wherein the source and drain electrodes overlap opposite end portions of the gate electrode, the semiconductor layer being exposed between the source and drain electrodes, and the gate electrode, the semiconductor layer, the source electrode and the drain electrode form a

thin film transistor;

forming a passivation layer over the data line, the source and drain electrodes, the data pad, the pixel connecting line, and the capacitor electrode;

forming a photoresist pattern on the passivation layer to cover the thin film transistor using a third mask process, the photoresist pattern having openings between the plurality of common electrode patterns and contact openings exposing the gate and data pads;

forming a transparent conductive layer on an entire surface of the substrate to cover the photoresist pattern; and

removing the transparent conductive layer on the photoresist pattern by stripping the photoresist pattern to obtain a pixel electrode, a gate pad terminal and a data pad termianl,

wherein the pixel electrode fits in the openings of the photoresist and directly contacts the pixel connecting line, the pixel electrode including a plurality of pixel electrode patterns,

wherein an innermost pixel electrode pattern has a substantially rod shape and other pixel electrode patterns are patterned to have semicircular shapes,

wherein an innermost portion of the plurality of common electrode patterns is substantially circular band shaped, and

wherein the aperture area is circular band shaped.

54. The method of claim 53, wherein the plurality of common electrode patterns are arranged in an alternating pattern with the plurality of pixel electrode patterns.

55. The method of claim 53, wherein the innermost pixel electrode pattern is disposed at a center portion of the pixel region where the common line and the pixel connecting line cross.

56. The method of claim 53, wherein the capacitor electrode pattern is connected to the thin film transistor though the pixel connecting line.

57. The method of claim 53, wherein the capacitor electrode overlaps the outermost common electrode pattern and forms a storage capacitor with the overlapped portion of the outermost common electrode pattern.

58. The method of claim 53, wherein the pixel and common electrode patterns are within the substantially rectangular opening except the outermost common electrode pattern.